REMARKS

The application has been carefully reviewed in light of the Final Office Action dated May 24, 2002. Claims 1-56 and 82-98 are pending in the application. Claims 38-56 are allowed. Claims 1-7, 16-19, 82 and 86-90 stand rejected under 35 U.S.C. §102(b) as being anticipated by Makihara et al. (US # 5,243,573). Claims 8, 11-13, 20, 23-33, 36-37, 83-85 and 91-98 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Maikihara et al. (US # 5,243,573) in view of Garcia (US # 5,949,259). Applicant respectfully traverses the rejection. Favorable reconsideration is requested.

Applicant has amended independent claims 1, 16, 26, 82 and 91 to more clearly define the meaning of the claim language. A marked up version of the amended claims appears in Appendix A. Applicant reiterates the arguments set forth in the response of March 11, 2002. It was previously explained that the present invention is an apparatus and method for adjusting clock skew. To reduce clock skew, a non-inverted clock signal ("CLK") and an inverted clock signal ("XCLK" – the complement) are connected to back-to-back inverters. The signal that takes longer to switch states (either CLK or XCLK) has an extra inverter driving it when it switches states and the signal that switches states faster has an extra inverter holding back the transition when it switches states. As a result, the "slower" signal (i.e., the one taking longer to switch states) and the "faster" signal are respectively altered relative to their transition times so that both signals effectively switch states at almost the same time (*see* specification page 12, lines 19 - page 14, lines 1-7; Fig. 4). The presently amended claims recite complementary clock signals, as well as the reduction in skew that results from the application of the presently claimed invention.

Makihara, however, is a circuit that senses the logic level of data signals output from a memory array. Unlike the present invention, which receives two complementary clock signals as inputs, and adjusts them to reduce the skew between them, Makihara senses the difference between a data signal and a reference data signal and outputs the recognized signal and its complement on two output lines. No skew adjustment is conducted in the disclosure. The portions cited by the Examiner (Fig. 2, etc.) discloses that the outputs N4 and N5 are being utilized to output a data signal and its complement (col. 2, lines 36-52; col. 3, lines 14-41); no input of complementary clock signals is disclosed. Furthermore, the Examiner's assertion that transistors 24-27 are configured to receive complementary clock signals as inputs is simply incorrect. There is nothing in the disclosure of Makihara teaching or suggesting such a configuration.

The Examiner asserted that the skew reduction element was not recited in the claims (Office Action 5/22/02, page 5, paragraph 5). This is incorrect. Claims 82 and 91 expressly recited "modifying the transition of one of said external clock signals relative to the other to produce from said external clock signals internal clock signals which have reduced skew." Applicant respectfully submits that this element is not taught or suggested in any of the cited art. Accordingly, the rejection as to claims 1-7, 16-19, 82 and 86-90 is improper and should be withdrawn.

Regarding the teachings in Garcia, there is nothing in the disclosure that teaches or suggests the input of complementary clock signals, nor is there any disclosure of reducing skew rates within the clock signals. Garcia does not cure the deficiencies of

Makihira. Accordingly, the rejections as to claims 8, 11-13, 20, 23-33, 36-37, 83-85 and 91-98 are also improper and should be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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APPENDIX A

Version With Markings to Show Changes Made

1. (Twice Amended) A circuit for reducing clock signal skew comprising:

at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second complementary clock output signals[;] , wherein the complementary clock input signals have a skewed time lag relative to each other;

first and second inverters each having an input and an output, said input of said first inverter connected to said output of said second inverter and to said first clock signal input/output line and said input of said second inverter connected to said output of said first inverter and to said second clock signal input/output line[.] , wherein the first and second inverters function to reduce the skew present in the complementary clock input signal.

16. (Twice Amended) A circuit for reducing clock signal skew comprising:

at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second internal complementary clock signals [;] , wherein the at least first and second complementary clock signals have a time lag skew relative to each other;

a first N-channel transistor coupled to a second N-channel transistor, a gate of said first N-channel transistor coupled to receive said second clock input signal, and said second N-channel transistor coupled to receive said first clock input signal;

a first P-channel transistor coupled to a second P-channel transistor, a gate of said first P-channel transistor coupled to receive said second clock input signal, and said second P-channel transistor coupled to receive said first clock input signal;

said second N-channel transistor coupled in series to said second P-channel transistor and said first clock signal input/output line connected between said second N-channel transistor and said second P-channel transistor; and

said first N-channel transistor coupled in series to said first P-channel transistor and said second clock signal input/output line connected between said first N-channel transistor and said first P-channel transistor[.] , wherein the transistors operate to output the at least first and second complementary clock signals with a reduced skew.

26. (Twice Amended) A circuit for reducing signal skew comprising:

at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second complementary clock output signals[;] , wherein the complementary clock input signals have a skewed time lag relative to each other;

first and second inverters each having an input and an output, said input of said first inverter connected to said output of said second inverter and to said first clock signal input/output line and said input of said second inverter connected to said output of said first inverter and to said second, complementary clock signal input/output line wherein the first and second inverters operate to reduce the skew present in the complementary clock

input signals; and a first and second driver circuit, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

82. (Amended) A method of generating an internal clock signal in an integrated circuit, the method comprising the steps of:

receiving first and second external clock signals, wherein the second external clock signal is an inverse of the first external clock signal and where there exists a time lag skew of one of said external clock signals relative to the other; and

modifying the transition of one of said external clock signals relative to the other to produce, from said external clock signals, internal clock signals, which have reduced skew.

91. (Amended) A method of generating an internal clock signal in an integrated circuit, the method of comprising the steps of:

receiving first and second external clock signals, wherein the second external clock signal is an inverse of the first external clock signal and where there exists a time lag skew of one of said external clock signals relative to the other;

buffering each of the first and second external clock signals using a reference voltage;

modifying the transition of one of said buffered external clock signals relative to the other to produce, from said buffered external clock signals, internal clock signals which have reduced skew.